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PROFESSIONAL SOFTWARE TOOLS FOR DEVICE MODELING

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ABSTRACT: In order to successfully design chips with higher integration and higher transmission speed, the work of modeling engineers to develop accurate device models up to tens of Gigahertz becomes more and more challenging. An absolute prerequisite for achieving this goal are accurate measurements, checked for data consistency, accurate instrument calibration, and correct de-embedding. Furthermore, today's high-frequency components require a lot of flexibility for the parameter extraction and device modeling process. Therefore, press-a-button solutions cannot provide the most accurately fitted model any more. It is required to have both, well educated modeling engineers and adequate software tools to obtain the required accurate design kits. Without this, high-frequency modeling can become quite time consuming, with a lot of guesswork and ad-hoc judgements, and, basically, not correct.

THE DEVICE MODELING PROCESS IN GENERAL

An idea of the general device modeling process is depicted in figure 1.

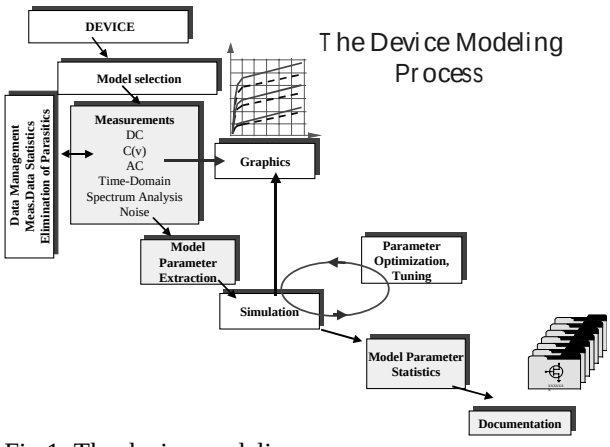

Fig.1: The device modeling process

For a given device, an adequate model is selected first. This can be a single model (like for transistors), or a composed sub-circuit consisting of standard devices. Next, the model equations, which are solved for the model parameters during model parameter extraction, give a clear indication about what kind of measurements and what type of stimulus sweeps are required for characterization. After all these measurements have been performed, the parameters of the selected model are reset. This means, the model becomes a very simple one: no bias dependency, and no frequency dependency. Then, during the parameter extraction process, more and more model parameters are extracted, and the selected model will fit more and more precisely the measured device. This extraction process is usually a combination of direct parameter determination out of the measured data, followed by parameter fine-tuning with an optimizer or interactively by the modeling engineer [1]. Once the parameter set has been obtained, its validity has to be checked and documented. Finally, the design kit is developed, allowing the design engineers to 'simply insert' this modeled component into their designs. And, of course, the better the model was developed, the easier can the design engineer realize his/her ultimate goal: a design, right the first time, with no further iterations.

FROM DC TO CV TO NWA

Figure 2 gives an impression of the basic modeling steps.

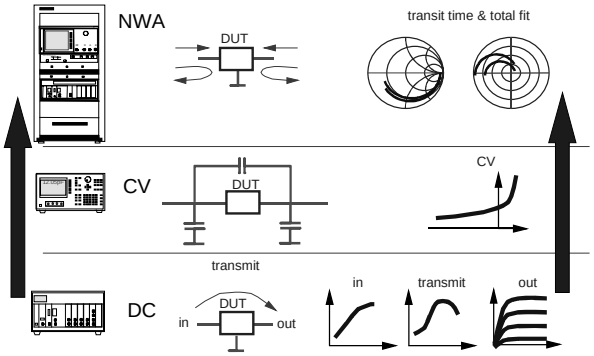

Fig.2: From DC to CV to S-parameters

For a general transistor modeling as an example, the measurement of the DC performance with respect to its input and output characteristics as well as its transfer function is done first, followed by the so-called CV modeling, i.e. the characterization of the depletion capacitances at 1MHz. Finally, the S-parameters of the transistor as well as of the dummy devices (contact capacitances and inductances) are measured [2 , 3].

After the de-embedding process has been verified (by modeling the THRU dummy device for example [1], the S-parameters are de-embedded (OPEN, SHORT dummy de-embedding)

After each step, the corresponding model parameters are extracted and fine-tuned. For the DC case, it is the non-linear model parameters, for the CV the junction capacitance parameters and for the S-parameters the transit time, and also the parasitics which are only visible at HF.

BEYOND S-PARAMETERS

However, we should keep in mind that the HF application of a device is not necessarily linear. While a S-parameter measurements by a network analyzer is usually performed at HF-signal levels below -30dBm (<1uW !), and while therefore modeling is based on these data, it must be checked if the model can also predict correctly the device performance above these low HF power levels. In most cases, spectrum analyzers will be involved, but also nonlinear network analyzers are available [4 - 6].

Figure 3 depicts this extension of modeling towards nonlinear HF.

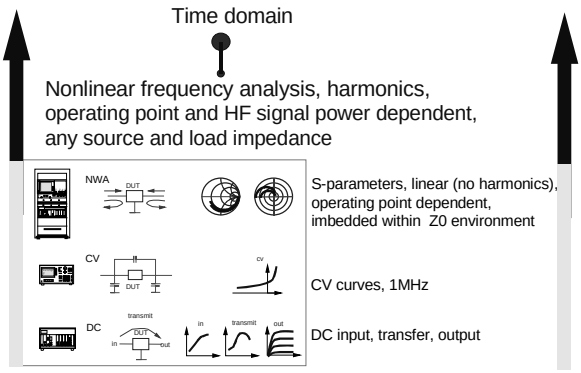

Fig.3: Beyond S-parameters

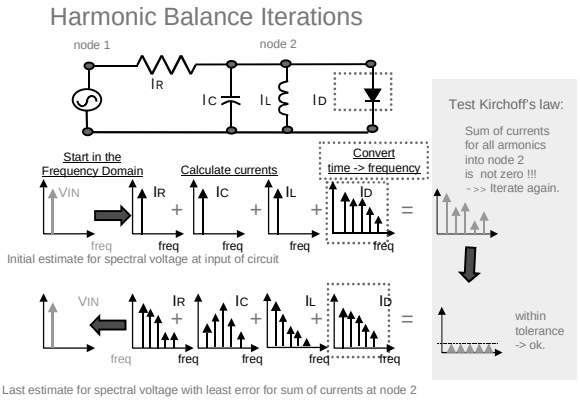

Fig.4: How harmonic balance simulators work

It should be noted that such kind of performance cannot be simulated using conventional SPICE-like simulators. Specific non-linear HF simulators like Agilent's ADS with harmonic balance simulation capabilities have to be applied. This kind of simulators does not need to perform any linearization in order to predict the HF performance. Applying a Fourier analysis, harmonic balance simulators 'balance the harmonics' at each node of the circuit in order to fulfill Kirchhoff's law that the sum of currents into a node is zero for all frequencies and for all HF power levels. Figure 4 shows how harmonic balance simulations work.

PARASITICS MODELING

Before we continue with considering the very device modeling, it should be noted that package, connector and board modeling becomes more and more important today. With the current clock rates of more than 1GHz, these unavoidable passive surroundings of the device can affect the overall performance so heavily that their influence cannot be neglected any more. As a final remark, such kind of modeling is performed using TDRs (time domain reflectometer) to characterize the pins or delay lines, while network analyzer (NWA) are used to model afterwards the cross-talk between these pins or lines.

TRANSISTOR MODELS: SCALING VS. NON-SCALING

Back to transistor modeling, we can distinguish between two kinds of models: scaling models and non-scaling. While scaling was included already in the very first MOS transistor models, it is still not fully implemented until today for bipolar transistors, see fig.5. On the other hand, bipolar models covered right from the beginning in the early 1970ies already HF performance, with the parameters for transit time for example. MOS, on the other side, reaches the GHz range only these days. Due to the incredible downsizing of the MOS components (allowing both, low power ***and*** high frequency performance), and the important economic fact that the combination of analog and digital devices, in the same technology, allow system-on-a-chip applications, makes MOS transistor these days more and more attractive and important.

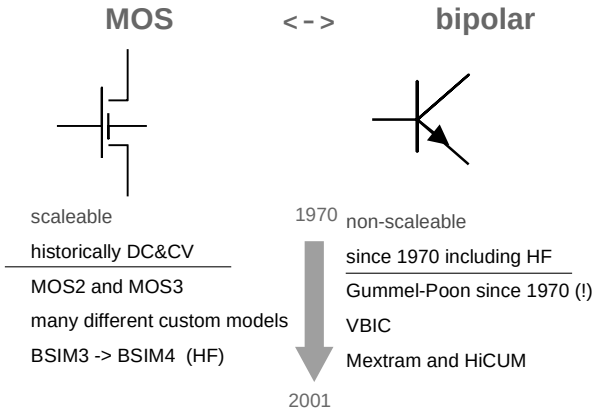

Fig.5: Transistor model development for MOS and bipolar

As an example for non-scaling modeling, figure 6 shows the so-called Gummel-Poon plot for a bipolar transistor and how some of the most important parameters can be extracted directly out of it.

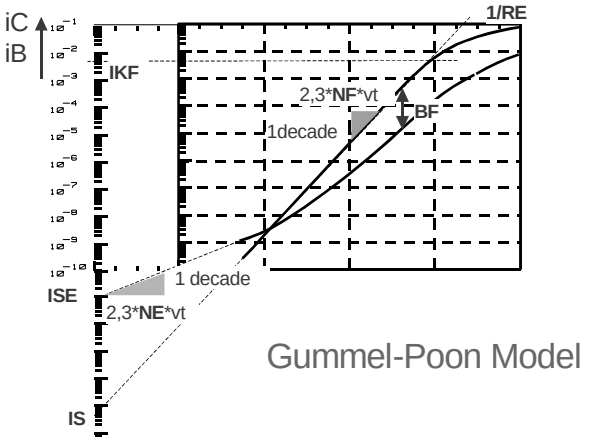

Fig.6: The Gummel-Poon model as a non-scaling model example

On the other side, as shown in figure 7, the modeling, i.e. parameter extraction for MOS transistors is generally quite different from that. After the most important parameters have been extracted from measurements of the biggest device, the shorter and more narrow device data are used *together* in order to find out the remaining, scaling model parameters.

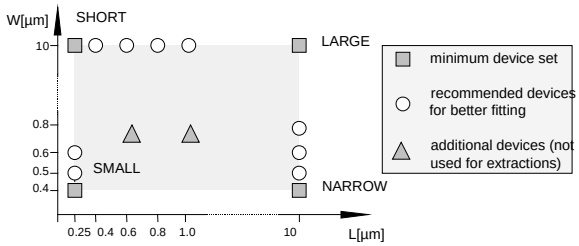

Fig.7: The BSIM3 model as a scaling model example

As can be seen in figure 8, the threshold parameters versus device length L are determined from a two-step procedure: first the threshold voltage (*not* the model parameter !) of every device geometry is extracted, and then, secondly, visualized in a separate plot, versus the scaling parameter length L. From this second plot, the several parameters, describing basically VTH = f(L,vB), are determined. This is called group device modeling strategy [7].

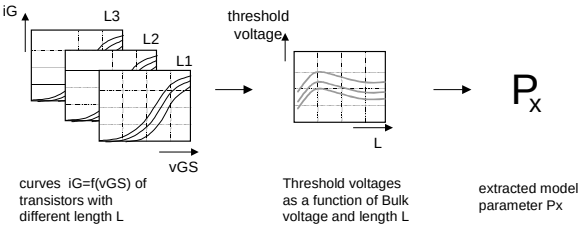

Fig.8: Group device extraction technique for scaled modeling

HF MODELING OF PASSIVE COMPONENTS

Besides transistors, passive components become more and more important when talking of system-on-a-chip devices. Mainly varactor diodes, spiral inductors, but also resistors etc. have to be modeled when applied in such HF circuits. In this case, the model consists of a sub-circuit, consisting of resistors, inductors and capacitors. Although many publications suggest a certain sub-circuit for a specific device, it was found that best modeling results can be achieved when developing a sub-circuit from the measured S-parameters, and then extract its model parameters [8].
Fig. 9 gives an example of modeling a spiral inductance on silicon, using a TEE schematic.

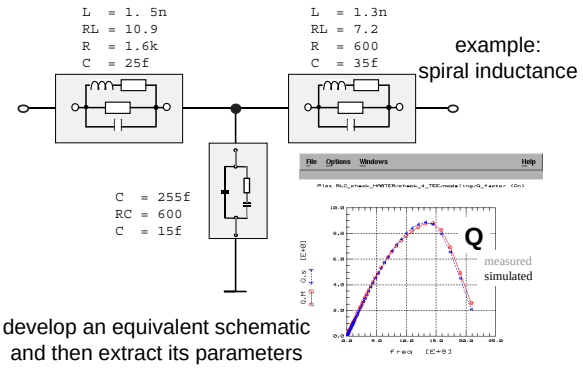

Fig.9: HF modeling of passive components

AUTOMATION: WAFER PROBING, AND SWITCHING MATRIX

Developing a model for an electrical device requires to first identify a 'golden' and also the boundary ±Sigma devices. Therefore, switching matrices and automated wafer probers are applied, see figure 10. These units also ease the measurements for scaleable devices like MOS transistors, allowing to use a probe card together with the switching matrix.

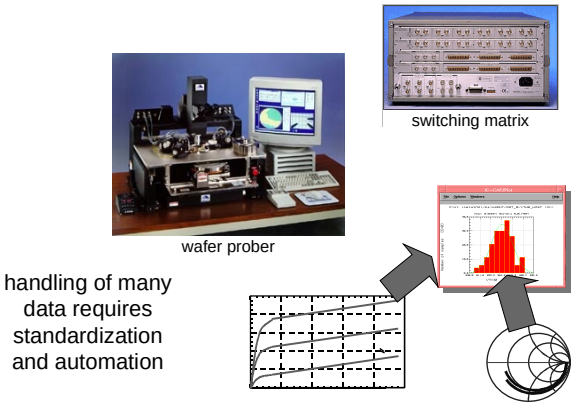

Fig.10: Automation: wafer probing and switching matrix

Because switching matrices have an upper limit frequency of some MHz, they are used for DC and CV measurements only. For HF measurements above some tens of MHz, up to tens of GHz, the network analyzers are connected directly to special HF probes (GSG ground-signal-ground). In this case, when performing measurements on scaling devices, a microstepping is performed by the wafer prober instead of using the switching matrix.

PROFESSIONAL MODELING SOFTWARE

For all the tasks described above, it is very helpful to use a dedicated control software. It serves to control the measurements, check the obtained results, to extract the model parameters, to interact with a simulator and, finally, to compare and optimize the simulated data versus the measured ones.

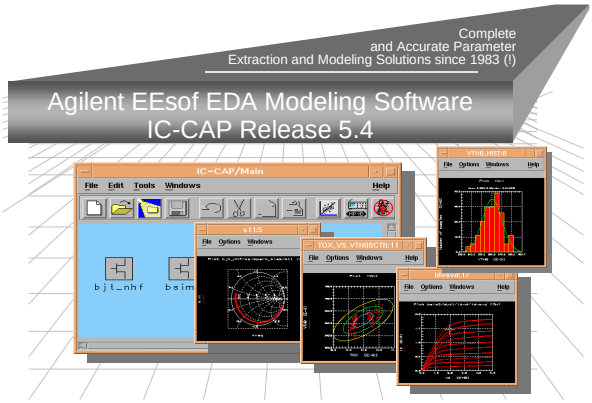

Fig.11: IC-CAP as an example for a professional commercial modeling software

The structure of such a tool is given in figure 12, showing the concept of Agilent's IC-CAP modeling software [9].

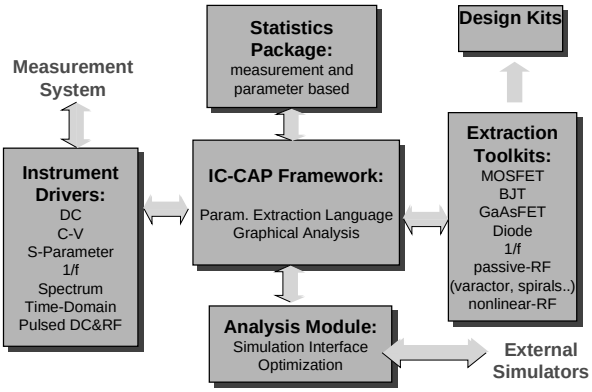

Fig.12: IC-CAP functionality structure

The core of any such software is to link the measurements to the simulations. In figure 13, we see how all kinds of measurement setups, from DC up to S-parameters and also including noise measurements (for transistors and passive HF components) are supported. Time domain instruments like oscilloscopes and time domain reflectometers (TDR) are supported to characterize large-scale components like packages, connectors and even printed circuit boards.

Also, a pulsed modeling system is available, allowing isothermal measurements with pulse widths down to 1us, and frequencies up to the GHz range. Such a tool is required to accurately model power devices, including self-heating effects.

On the other hand, the link to several industry-standard simulators allows to compare the device measurements with the simulations of the same kind like used later in the design phase. This means that which such a basic concept, all kinds of devices, which can be described by the selected simulator by either a single model or by a more complex sub-circuit, can be modeled. This is even true for custom models, integrated int he

simulator. For this purpose, open extraction routines, easily modifiable and easily enhanceable by the user, are mandatory for flexible and accurate modeling. In the case of IC-CAP, an interpreter language, comparable to BASIC, is included to allow such kind of custom modeling.

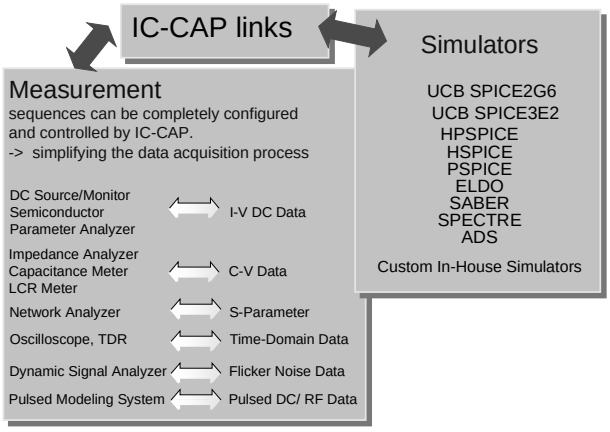

Fig.13: Linking measurements with simulators

Examples of devices, modeled with such a software concept are:

diode
MOS, bipolar, HBT, HEMT transistors
operational amplifiers
varactors, inductors, vias
packages, connectors, circuit boards

CONCLUSION

The use of professional tools is a prerequisite to develop accurate device models, from DC to GHz, including noise modeling and nonlinear HF effects, within a reasonable time. With technology going faster and faster towards ultra-high frequencies, circuit designs can only be accurate and right-the-first-time if the underlying device models are accurately modeled with physically meaningful model parameters.

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